IN THE CLAIMS

1. (Original) A circuit board, comprising:

a first conductive layer including a first interstice;

a second conductive layer including a second interstice engaged with the first interstice; and

a dielectric layer disposed between the first interstice and the second interstice.

2. (Original) The circuit board of Claim 1, wherein the first conductive layer is a first power plane of the circuit board.

3. (Original) The circuit board of Claim 2, wherein the second conductive layer is a second power plane of the circuit board.

4. (Original) The circuit board of Claim 2, wherein the second conductive layer is a ground plane of the circuit board.

5. (Original) The circuit board of Claim 1, wherein the first and second conductive layers are horizontally-opposed.

6. (Original) The circuit board of Claim 1, wherein the first and second conductive layers are vertically-overlapping.

7. (Withdrawn) The circuit board of Claim 1, wherein the first and second interstices are formed in a non-complementary shape.

8. (Original) A circuit board, comprising:

a first conductive layer sinuously intertwined with a second conductive layer; and

a dielectric layer disposed between the first conductive layer and the second conductive layer, wherein the dielectric layer has a dielectric constant of about 2 to about 11.

9. (Original) The circuit board of Claim 8, wherein the dielectric layer is selected from a group consisting of fluororesins, polynorbornene resins, benzocyclobutene resins, polyimide resins, and epoxy resins.

10. (Original) The circuit board of Claim 8, wherein the first and second conductive layers are horizontally-opposed.

11. (Original) The circuit board of Claim 8, wherein the first and second conductive layers are vertically-overlapping.

12. (Withdrawn) A circuit board, comprising:

a first conductive layer including a first interstice and a third interstice;

a second conductive layer including a second interstice engaged with the first interstice, and a fourth interstice engaged with the third interstice; and

a dielectric layer disposed between the first and third interstices, and the second and fourth interstices.

13. (Withdrawn) The circuit board of Claim 12, wherein the first and second interstices are formed in a complementary shape.

14. (Withdrawn) The circuit board of Claim 12, wherein the first and second interstices are formed in a complementary rectangular shape.

15. (Withdrawn) The circuit board of Claim 12, wherein the first and second interstices are formed in a non-complementary shape.

16. (Withdrawn) A circuit board, comprising:

a first conductive layer sinuously intertwined with a second conductive layer; and

a dielectric layer disposed between the first conductive layer and the second conductive layer, wherein the first and second conductive layers are formed in a complementary circular shape.

17. (Withdrawn) A circuit board, comprising:

a first conductive layer sinuously intertwined with a second conductive layer; and

a dielectric layer disposed between the first conductive layer and the second conductive layer, wherein the first and second conductive layers are formed in a complementary spiral shape.

18. (Withdrawn) A circuit board, comprising:

a first conductive layer including a first interstice, wherein the first interstice has a single first width laying in a first plane;

a second conductive layer including a second interstice engaged with the first interstice, wherein the second has a single second width laying in a second plane; and

a dielectric layer disposed between the first and second interstices, wherein the first and second planes are substantially parallel, and wherein the first width substantially overlaps the second width.

19. (Original) A circuit board, comprising:

a first conductive layer including a first interstice, wherein the first interstice has a plurality of first widths laying in a first plane;

a second conductive layer including a second interstice engaged with the first interstice, wherein the second interstice has a plurality of second widths laying in a second plane; and

a dielectric layer disposed between the first and second interstices, wherein the first and second planes are substantially parallel, and wherein each one of the first plurality of widths substantially overlaps at least one of the second plurality of widths.

20. (Original) A circuit board, comprising:

a first conductive layer including a first interstice, wherein the first interstice has a plurality of first width laying in a first plane;

a second conductive layer including a second interstice engaged with the first interstice, wherein the second has a single second width laying in a second plane; and

a dielectric layer disposed between the first and second interstices, wherein the first and second planes are substantially parallel, and wherein the second width substantially overlaps at least one of the first plurality of widths.

21. (Original) A circuit board, comprising:

a first conductive layer including a plurality of grooves;

a second conductive layer including a plurality of tongues, wherein each one of the plurality of grooves is engaged with at least one of the plurality of tongues; and

a dielectric layer disposed between the plurality of grooves and the plurality of tongues.

22. (Original) The circuit board of Claim 21, wherein the plurality of grooves and the plurality of tongues are formed in a complementary rectangular shape.

23. (Withdrawn) The circuit board of Claim 21, wherein each one of the plurality of grooves includes an increasing depth, and wherein each one of the plurality of tongues includes a complementary increasing length.

24. (Original) The circuit board of Claim 21, wherein the first conductive layer is a first power plane of the circuit board and the second conductive layer is a second power plane of the circuit board.

25. (Original) The circuit board of Claim 21, wherein each one of the plurality of grooves has a depth, and wherein each one of the plurality of tongues overlaps at least one of the first plurality of grooves by at least about 5 percent of the depth.

26. (Original) The circuit board of Claim 21, wherein the first and second conductive layers are horizontally-opposed.

27. (Original) The circuit board of Claim 21, wherein the first and second conductive layers are vertically-overlapping.

28. (Original) A circuit board having a first conductive layer and a second conductive layer, wherein the first conductive layer includes a first interstice and the second conductive layer includes a second interstice, the circuit board comprising:

a capacitor having a dielectric layer disposed between the first interstice and the second interstice, wherein the first interstice is engaged with the second interstice.

29. (Original) The circuit board of Claim 28, wherein the dielectric layer has a dielectric constant of about 2 to about 11.

30. (Original) The circuit board of Claim 28, wherein the dielectric constant is about 3 to about 5.

31. (Original) The circuit board of Claim 28, wherein the first interstice has a depth, and wherein the second interstice is engaged with the first interstice such that the first and second interstices overlap by about 5 percent to about 99 percent of the depth.

32. (Original) The circuit board of Claim 28, wherein the first and second conductive layers are horizontally-opposed.

33. (Original) The circuit board of Claim 28, wherein the first and second conductive layers are vertically-overlapping.

34. (Original) A circuit board having a first conductive layer and a second conductive layer, wherein the first conductive layer includes a first interstice and the second conductive layer includes a second interstice, the circuit board comprising:

a capacitor having a dielectric layer disposed between the first interstice and the second interstice, wherein the first interstice is engaged with the second interstice, and wherein the first conductive layer is connected to a first power supply voltage; and

an electrical circuit mounted to the circuit board, wherein the electrical circuit is powered by the first power supply voltage.

35. (Original) The circuit board of Claim 34, wherein the second conductive layer is connected to a second power supply voltage, and wherein the electrical circuit is powered by the second power supply voltage.

36. (Original) The circuit board of Claim 34, wherein the dielectric layer has a dielectric constant chosen to provide a preselected amount of capacitance between the first and second conductive layers.

37. (Original) The circuit board of Claim 34, wherein a degree of overlap between the first and second interstices is chosen to provide a preselected amount of capacitance for the capacitor.

38. (Original) An electronic circuit, comprising:

a first power terminal operationally connected to a first conductive layer having a first interstice;

a second power terminal operationally connected to a second conductive layer having a second interstice engaged with the first interstice; and

a dielectric layer disposed between the first interstice and the second interstice.

39. (Original) The electronic circuit of Claim 38, wherein the first and second conductive layers are horizontally-opposed.

40. (Original) The electronic circuit of Claim 38, wherein the first and second conductive layers are vertically-overlapping.

41. (Withdrawn) The electronic circuit of Claim 40, wherein the first interstice has a single first width laying in a first plane and the second interstice has a single second width laying in a second plane, wherein the first and second planes are substantially parallel, and wherein the first width substantially overlaps the second width.

42. (Original) The electronic circuit of Claim 40, wherein the first interstice has a plurality of first widths laying in a first plane and the second interstice has a plurality of second widths laying in a second plane, wherein the first and second planes are substantially parallel, and wherein each one of the first plurality of widths substantially overlaps at least one of the second plurality of widths.

43. (Original) The electronic circuit of Claim 40, wherein the first interstice has a plurality of widths laying in a first plane and the second interstice has a second width laying in a second plane, wherein the first and second planes are substantially parallel, and wherein the second width substantially overlaps at least one of the plurality of widths.

44. (Original) A power supply system, comprising:

a first power supply having a first power terminal and a first ground terminal, wherein the first power terminal is operationally connected to a first conductive layer of a circuit board, wherein the first conductive layer includes a first interstice;

a second power supply having a second power terminal and a second ground terminal, wherein the first ground terminal is operationally connected to the second ground terminal, and wherein the second power terminal is operationally connected to a second conductive layer of the circuit board, the second conductive layer including a second interstice engaged with the first interstice; and

a dielectric layer disposed between the first interstice and the second interstice.

45. (Original) A memory circuit module, comprising:

a circuit board including a power plane having a first interstice and a ground plane having a second interstice engaged with the first interstice, wherein a dielectric layer is disposed between the first and second interstices; and

a memory chip having a power terminal connected to the power plane and a ground terminal connected to the ground plane.

46. (Original) A computer system, comprising:

a circuit board comprising:

a first conductive layer including a first interstice;

a second conductive layer including a second interstice engaged with the first interstice;

a dielectric layer disposed between the first interstice and the second interstice; and

a processor connected to the first and second conductive layers.

47. (Original) The computer system of Claim 46, wherein the first and second interstices are formed in a complementary shape.

48. (Original) The computer system of Claim 46, wherein the first and second interstices are formed in a complementary rectangular shape.

49. (Withdrawn) The computer system of Claim 46, wherein the first and second interstices are formed in a non-complementary shape.

50. (Original) A method of forming a circuit board having a first conductive layer and a second conductive layer, comprising:

forming a first interstice in the first conductive layer;

forming a second interstice in the second conductive layer;

inserting a dielectric layer between the first and second interstices; and

engaging the first and second interstices.

51. (Original) The method of Claim 50, further comprising:

selecting the dielectric layer to have a dielectric constant of between about 2 and about 11.

52. (Original) The method of Claim 50, further comprising:

selecting the dielectric layer to have a dielectric constant which provides a preselected amount of capacitance between the first and second conductive layers.

53. (Original) The method of Claim 50, wherein the first interstice has a depth, and wherein engaging the first and second interstices further comprises:

engaging the first and second interstices such that the first interstice is overlapped by the second interstice by about 5 percent to about 99 percent of the depth.

54. (Original) The method of Claim 50, wherein the first interstice has a depth, and wherein engaging the first and second interstices further comprises:

selecting a degree of overlap between the first and second interstices so as to provide a preselected amount of capacitance between the first and second conductive layers.

55. (Original) A method of forming a circuit board having a first conductive layer and a second conductive layer, comprising:

selecting a first shape for a first interstice in the first conductive layer;

selecting a second shape for a second interstice in the second conductive layer;

forming a dielectric layer;

forming the first conductive layer on the dielectric layer;

forming the first interstice in the first conductive layer;

forming the second conductive layer on the dielectric layer;

forming the second interstice in the second conductive layer; and

sinuously intertwining the first and second interstices.

56. (Original) The method of Claim 55, wherein selecting the first shape and the second shape includes selecting shapes that are complementary.

57. (Original) The method of Claim 55, wherein selecting the first shape and the second shape includes selecting shapes that are circular.

58. (Original) The method of Claim 55, wherein selecting the first shape and the second shape includes selecting shapes that are spirals.

59. (Original) The method of Claim 55, wherein selecting the first shape and the second shape includes selecting shapes that are non-complementary.

60. (Original) A method of forming a circuit board having a first conductive layer and a second conductive layer, comprising:

forming a plurality of grooves in the first conductive layer;

forming a plurality of tongues in the second conductive layer;

inserting a dielectric layer between the plurality of grooves and the plurality of tongues; and

engaging the plurality of grooves with the plurality of tongues.

61. (Original) A method of forming a capacitor having a dielectric layer in a circuit board having a first conducting layer and a second conducting layer, comprising:

forming a first interstice in the first conductive layer;

forming a second interstice in the second conductive layer, wherein the second interstice engages the first interstice; and

inserting the dielectric layer between the first and second interstices.

62. (Original) A method of forming a capacitor having a dielectric layer in a circuit board having a first conducting layer and a second conducting layer, comprising:

forming a dielectric layer;

forming the first conductive layer on the dielectric layer;

forming a first interstice in the first conductive layer;

forming a second conductive layer on the dielectric layer; and

forming a second interstice in the second conductive layer, wherein the second interstice engages the first interstice.

63. (Original) A method of forming a circuit module using a memory chip and a circuit board, comprising:

forming a first interstice in a power plane of the circuit board;

forming a second interstice in a ground plane of the circuit board, wherein the second interstice engages the first interstice;

disposing a dielectric layer between the first and second interstices;

connecting a power terminal of the memory chip to the power plane; and

connecting a ground terminal of the memory chip to the ground plane.

64. (Original) A method of assembling a computer system, comprising:

connecting a memory module to a circuit board including a processor, wherein the circuit board comprises:

a first conductive layer including a first interstice;

a second conductive layer including a second interstice engaged with the first interstice; and

a dielectric layer disposed between the first interstice and the second interstice.

65. (New) A circuit board having a first conductive layer and a second conductive layer, comprising:

means for forming a first interstice in the first conductive layer;

means for forming a second interstice in the second conductive layer;

means for inserting a dielectric layer between the first and second interstices; and

means for engaging the first and second interstices.